# A FAST FORWARDING ALU

## ABSTRACT OF THE DISCLOSURE

An apparatus and method for performing fast arithmetic operations, including addition, in a pipelined circuit is described. The apparatus and method operating on a first binary number and a second binary number comprise: a first arithmetic logic unit (ALU) operating on a first lower portion of the first binary number and a second lower portion of the second binary number to produce a first result and a carry out signal; and a second ALU operating on a first upper portion of the first binary number and a second upper portion of the second binary number to produce a second result; wherein at least a portion of the pipelined circuit stalls in response to the carry out signal. Another embodiment includes memory comprising a plurality of words, each word comprising data bits and a flag bit indicating a predetermined number of the most significant data bits are all zero.